20/Appeal Brief T.Steptoe 6-11-03

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Jiang et al.

Serial No.: 09/483,712

Filed: January 14, 2000

For: CHIP-SCALE PACKAGES HAVING ENCAPSULATED CARRIER BONDS (as amended)

Confirmation No.: 8743

Examiner: M. Warren

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BRIEF ON APPEAL

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is in furtherance of the Notice of Appeal, filed in this case on March 27, 2003, and is submitted in TRIPLICATE pursuant to 37 C.F.R.§ 1.192(a) and in the format required by 37 C.F.R. § 1.192(c) and with the fee required by 37 C.F.R. § 1.17(c):

1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc., the assignee of the pending application as recorded with the United States Patent and Trademark Office on January 14, 2000, at Reel 010532, Frame 0640.

2) RELATED APPEALS AND INTERFERENCES

Neither Appellants, Appellants' representative, nor Assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

3) STATUS OF CLAIMS

Claims 1 through 29 are pending in the application.

Claims 21 through 29 have been withdrawn from consideration.

Claims 1 through 20 stand rejected.

No claims are allowed.

The rejections of claims 1 through 20 are being appealed.

4) STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed on December 31, 2002. On February 5, 2003, the Applicants filed Remarks under 37 C.F.R. § 1.116 in response to the Examiner's remarks in the Final Office Action of December 31, 2002. No amendments were proposed in the Remarks. An Advisory Action mailed on March 18, 2003 found the Applicants' arguments in the Remarks unpersuasive and maintained the rejection of claims 1 through 20.

5) SUMMARY OF THE INVENTION

The invention presently claimed in pending claims 1 through 20 relates to chip-scale semiconductor packages and, more specifically, to low cost chip-scale semiconductor packages in a ball grid array configuration using a lead frame as an interposer. (Specification, at page 2, lines 6-9.)

One embodiment of a chip-scale package according to the present invention comprises a semiconductor die having bond pads on the active surface thereof (Drawings, FIG. 3, elements 10, 11, and 12), and conductive traces such as lead fingers (Drawings, FIG. 3, element 14) attached to the active surface with a dielectric adhesive (Drawings, FIG. 3, element 21. (Specification, at page 6, lines 22-23.) The dielectric adhesive may comprise a polyimide film or a dielectric tape. (Specification, at page 6, lines 23-26.) The bond pads of the semiconductor die are connected to the lead fingers by discrete conductive bonds such as wire bonds (Drawings, FIG. 3, element 16), and discrete conductive elements such as solder balls (Drawings, FIG. 3, element 18) are secured to the lead fingers. (Specification, at page 6, lines 14-17). The assembly is encapsulated within an encapsulant material (Drawings, FIG. 3, element 60), but for the protruding outer ends of the discrete conductive elements. (Specification, at page 6, line 26 to page 7, line 2.)

In a further embodiment of the chip-scale package, carrier bonds (Drawings, FIG. 4, element 50) attached to the lead fingers (Drawings, FIG. 4, element 20) may comprise solder balls or conductive resins or polymers containing conductive particles. (Specification, at page 8, lines 21-24.) The bond pads of the semiconductor die are connected to the lead fingers by bonding techniques such as wire bonds, TAB bonding or thermocompression bonding. (Specification, at page 8, lines 9-15.)

In yet a further embodiment of the chip-scale package, the discrete conductive elements or carrier bonds may be attached along the span of the lead fingers in alternative patterns (Drawings, FIG. 5, elements 50A, 50B, and 50C). (Specification, at page 9, lines 15-20.)

6) ISSUE

Whether claims 1 through 20 are patentable under 35 U.S.C. § 103(a) over Farnworth (United States Patent No. 6,147,413) in view of Lee et al. (United States Patent No. 5,894,107).

7) GROUPING OF CLAIMS

Appellants submit that the group of claims 1, 2, 4, 5, 7 through 10, 13, and 15 through 20 stand and fall together for purposes of this appeal. It is further submitted that claims 3, 6, 11, 12, and 14, which depend from claim 2, do not stand and fall with claim 2 or with any other claims of the above group, as each are separately patentable for the reasons set forth in Section 8(C)(4).

8) ARGUMENT

A. Authorities Relied Upon

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior

art, and not based on Applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

It is improper to combine references where the references teach away from their combination. MPEP § 2145 (citing *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)).

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert.denied*, 469 U.S. 851 (1984).

The Federal Circuit has repeatedly cautioned against employing hindsight by using the applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teaching of the prior art. *See, e.g., Grain Processing Corp. v. American-Maize Prods. Co.*, 840 F.2d 902, 907, 5 U.S.P.Q.2d 1788, 1792 (Fed. Cir. 1988).

B. Summary of Cited Prior Art

Farnworth describes a method of forming conductive bumps on a die for flip chip type attachment using simplified masking steps. In the method, a first polyamide passivation layer 1006 is applied to a wafer active surface 1010 by spin coating (col. 4, lines 3-10). A via 1008 is etched through passivation layer 1006 to expose bond pad 1002 (col. 4, lines 27-32). A conductive layer 1012 is then deposited over passivation layer 1006 and masked and etched to form repattern trace 1016 which extends to an alternative bond pad location (col. 4, lines 39-44). A second passivation layer 1018 is spun-on over repattern trace 1016, and a via 1026 is formed therein to connect a solder ball 1032 to the alternative bond pad location of repattern trace 1016 (col. 4, line 45 - col. 5, line 40).

Lee et al. teaches a prior art chip-size package that uses half etched leads 76 to connect to bonding pads 74. (Fig. 1 and cols. 1 and 2). Leads 76 are attached to an

active surface of semiconductor chip 72 by adhesive tape 78, and bonding pads 74 are connected to leads 76 with wires 80 (col. 1, line 66 - col. 2, line 1). The assembly is encapsulated with epoxy molding compound 82 such that bonding pads 74 and wires 80 are protected from the external environment, while the thick portions of leads 76 are exposed to the outside (col. 2, lines 1-8).

C. Arguments for Patentability of Claims 1 through 20

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In rejecting claims 1 through 20, the Office asserts that Farnworth discloses all of the elements of the claims except the discrete conductive bond. The Office then concludes that it would be obvious to combine Lee et al. with Farnworth, and that Lee et al. is "only cited to teach the well known discrete bond." (Office Action mailed 12/31/2002, paper no. 16 at page 4, lines 7-8.) The fact that bond wires such as those taught by Lee et al. are known in the art, does not mean that bond wires may be incorporated into the structure disclosed by Farnworth. Instead, Applicants respectfully submit that combining Farnworth and Lee et al. in such a manner is improper and does not satisfy the requirements of an obviousness-type rejection under 35 U.S.C. § 103(a) for several reasons.

(1) *There is no motivation for one of ordinary skill in the art to combine the references as suggested by the Office*:

First, the Office suggests that it would be obvious to "modify the conductive trace configuration of Farnworth by employing a lead on chip configuration as taught by Lee to increase the package density and provide better electrical performance." Due to the differences in structure and scale between the repattern traces of Farnworth and the wires of Lee et al., Applicants submit there is no support for this line of reasoning.

Farnworth is directed generally to repatterning of flip chip or BGA type bond locations on a semiconductor die and more specifically to forming the repattern traces with reduced masking steps (col. 1, lines 14-22). Contrary to the suggestion of the Office, employing the bond wires of Lee et al. with the repattern structures of Farnworth would not increase package density. Repattern traces for flip chip or BGA structures as described in Farnworth are formed by masking and etching an under bump metallization that is adhered in a thin layer to the surface of the underlying passivation layer (col. 4, lines 33-44). Bond wires used in lead on chip configurations, on the other hand, are well known as extending between bonding locations in elevated, arched configurations (see Lee et al, Fig. 1). Adding bond wires to the repattern structure of Farnworth would, therefore, **require an enlarged packaged size** to accommodate the height of the bond wires within the passivation layer 1018.

Furthermore, bond wires would not provide better electrical performance, as suggested by the Office, but would instead **decrease electrical performance**. The bond wires would add length to the conductive pathway between bond pad 1002 and solder ball 1032, thereby increasing electrical resistance and the possibility of interference from inductance generated signal noise. It is also well known in the art that attaching bond wires is difficult and must be carried out under tightly controlled processing conditions. Adding bond wires to the repattern structure of Farnworth would raise the possibility of improper bond wire attachment degrading the electrical performance.

(2) *The references teach away from the proposed combination*:

Moreover, Applicants respectfully submit that Farnworth teaches away from any combination with Lee et al. Farnworth indicates an object of the invention is to simplify or eliminate masking steps in UBM pad forming when repatterning bond pad locations (Abstract and col. 1, lines 14-22). In its present form, the invention described by Farnsworth allows the repattern trace 1016 connecting bond pad 1002 and solder ball 1032 to be formed with a single mask and etch step (col. 4, lines 39-44). In order to include an intermediate bond wire between repattern trace 1016 and bond pad 1002, **additional or more complicated masking steps would be required**. Further process steps would also be necessary in terms of connecting trace 1016 and bond pad 1002 with a bond wire instead of directly connecting them.

It is improper to combine references where the references teach away from their combination. MPEP § 2145 (citing *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)). Furthermore, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert.denied*, 469 U.S. 851 (1984).

In sum, there is no reasonable basis for why one of ordinary skill in the art would be motivated to modify the repattern structure of Farnworth with the bond wires of Lee et al., when doing so would increase the package size, reduce performance and complicate the formation process. Rather than presenting a valid motivation for the above combination, Applicants respectfully submit that the Office has merely attempted to piece together the claimed invention with the hindsight benefit of Applicants' own disclosure. The Federal Circuit has repeatedly cautioned against employing hindsight by using the applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teaching of the prior art. *See, e.g., Grain Processing Corp. v. American-Maize Prods. Co.*, 5 U.S.P.Q.2d 1788, 1792 (Fed. Cir. 1988).

(3) *There is no reasonable expectation of success*:

Even if some motivation could be found for adding bond wires to the structure of Farnworth, there is no reasonable expectation of success for the combination, as the trace formation process used in Farnworth is not compatible with bond wires. As described above, Farnworth uses a series of mask, etch and spin coat steps to form via 1008 and repattern trace 1016 and to cover the trace configuration with passivation layer 1018 (Farnworth at col. 4). It is unclear how these steps could be carried out in the presence of bond wires. At the least, the process described by Farnworth **would require major alterations to provide the proposed combination**, rendering it non-obvious.

(4) *The cited references do not teach or suggest all of the claim limitations*:

Finally, Claims 3, 6, 11, 12, and 14 are further patentable because the combination of Farnworth and Lee et al. as presented by the Office does not teach or suggest all the claim limitations. Claim 3, for instance, recites the limitation "wherein said dielectric element includes an adhesive-coated polyimide tape." Farnworth, on the other hand, does not disclose an adhesive-coated polyimide tape, but instead uses a polyamide layer 1006 applied by spin coating (col. 4, lines 1-26). Likewise, claim 6 recites that "said plurality of conductive traces comprises lead fingers." The repattern traces of Farnworth are not comprised of lead fingers, but instead comprise a conductive layer 1012 of solder wettable metal applied over polyamide layer 1006 and etched into repattern traces 1016 (col. 4, lines 33-48). Claims 11 and 12 further recite discrete conductive elements comprised of "TAB bonds" or "thermocompression bonds." Farnworth does not disclose such structures. Claim 14 recites a plurality of carrier bonds comprised of a "conductive or conductor-filled polymer." Farnworth is limited to a description of a solder ball 1032 (col. 5, lines 38-40). The citation of Lee et al. to add bond wires to the repattern structure of Farnworth does not overcome these deficiencies.

In view of the foregoing, Applicants respectfully submit that the combination of Farnworth with Lee et al. fails to establish a *prima facie* case of obviousness with respect to claims 1 through 20 under 35 U.S.C. § 103(a).

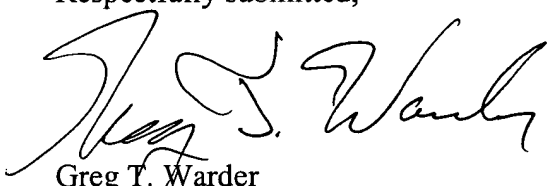
9) APPENDICES

A copy of claims 1 through 20, as amended, is appended hereto as "Appendix A."

10) CONCLUSION

Applicants respectfully request the reversal of the rejections of currently pending claims 1 through 20 for the reasons set forth above.

Respectfully submitted,



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APPENDIX A

1. (Previously Twice Amended) A chip-scale package comprising:

a semiconductor die having an active surface having at least one bond pad thereon;

at least one conductive trace spaced from said at least one bond pad and having an upper surface and a lower surface, the lower surface of said at least one conductive trace substantially non-conductively attached to a portion of the active surface of said semiconductor die;

at least one discrete conductive bond connecting the at least one conductive trace to the at least one bond pad on the active surface of said semiconductor die;

at least one carrier bond attached to the upper surface of the at least one conductive trace; and

an encapsulant material encapsulating said semiconductor die, the at least one conductive trace, the at least one discrete conductive bond and a portion of the at least one carrier bond, the at least one carrier bond having another portion extending beyond said encapsulant material.

2. (Previously Three Times Amended) A chip-scale package comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon;

a dielectric element having an upper surface and a lower surface, the lower surface of said dielectric element attached to a portion of the active surface of said semiconductor die;

a plurality of conductive traces spaced from said plurality of bond pads, each trace of the plurality of conductive traces having an upper surface and a lower surface, the lower surface of each trace of said plurality of conductive traces attached to a portion of the upper surface of said dielectric element for connecting each conductive trace of said plurality of conductive traces to the active surface of said semiconductor die;

a plurality of discrete conductive bond members, at least one discrete conductive bond member of the plurality of conductive bond members connecting each conductive trace of said plurality of conductive traces to at least one bond pad of the plurality of bond pads on the active surface of said semiconductor die;

a plurality of conductive carrier bonds, at least one carrier bond of the plurality of conductive carrier bonds disposed on the upper surface of each conductive trace of said plurality of conductive traces; and

an encapsulating material disposed about at least portions of said semiconductor die, said dielectric element, said plurality of conductive traces, said plurality of discrete conductive bond members and a portion of each carrier bond of said plurality of conductive carrier bonds.

3. (Original) A chip-scale package as in claim 2, wherein said dielectric element includes an adhesive-coated polyimide tape.

4. (Original) A chip-scale package as in claim 2, wherein said dielectric element includes a polyimide film.

5. (Original) A chip-scale package as in claim 2, wherein the upper surface and lower surface of said dielectric element are attached respectively to a portion of the lower surface of each conductive trace of said plurality of conductive traces and a portion of the active surface of said semiconductor die connecting portions of said plurality of conductive traces and portions of said semiconductor die.

6. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive traces comprises a plurality of lead fingers.

7. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive traces comprises a conductive metal.

8. (Previously Twice Amended) A chip-scale package as in claim 2, wherein said plurality of discrete conductive bond members comprises a conductive metal.

9. (Previously Twice Amended) A chip-scale package as in claim 2, wherein said plurality of discrete conductive bond members comprises bond wires.

10. (Original) A chip-scale package as in claim 9, wherein said bond wires comprise gold or aluminum.

11. (Previously Twice Amended) A chip-scale package as in claim 2, wherein said plurality of discrete conductive bond members comprises TAB bonds.

12. (Previously Twice Amended) A chip-scale package as in claim 2, wherein said plurality of discrete conductive bond members comprises thermocompression bonds.

13. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds includes metal.

14. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds comprises a conductive or conductor-filled polymer.

15. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds is selectively located on the upper surface of said plurality of conductive traces forming an array.

16. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds comprises solder balls.

17. (Original) A chip-scale package as in claim 2, wherein said encapsulating material comprises a substantially non-conductive material.

18. (Original) A chip-scale package as in claim 2, wherein said encapsulating material comprises a material having a low modulus of elasticity.

19. (Previously Amended) A chip-scale package as in claim 2, wherein each conductive carrier bond of said plurality of conductive carrier bonds further comprises an upper portion and a lower portion, said lower portion of a conductive carrier bond attached to the upper surface of a conductive trace of said plurality of conductive traces.

20. (Previously Amended) A chip-scale package as in claim 19, wherein said encapsulating material is disposed about the lower portions of said plurality of conductive carrier bonds.